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# Strain mapping of transistor structures in a 22nm Fully Depleted Silicon-On-Insulator technology

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**Strain mapping of transistor structures in a 22nm Fully Depleted Silicon-On-Insulator technology**

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With the advent of the Big Data and 5G era, modern electronic devices are needed to be operated with low energy consumption, high performance, and manufactured at low cost. One of potential IC technologies candidates is 22FDX offered by GLOBALFOUNDRIES that utilizes a fully depleted silicon-on-insulator (FDSOI) technique. FDSOI employs a thin buried oxide layer to form an ultra-thin channel so that short-channel effects can be mitigated and parasitics of such devices can also be reduced comparing to bulk CMOS technology. Speed and power consumption of devices are improved accordingly.
Introducing mechanical strain to transistor channels e.g. by epitaxial growth or process induced pre-stressed overlayers or periphery layouts alters the crystal lattice and thus also the band structure of the semiconducting channel. Therefore such changes in the energy band may also lead to the alteration of the carrier mobility. With the proper strain introduced to N- and P-type transistors, device performance can consequently be improved even for their RF capability, especially in FDSOI technology due to its thin thickness of the channel.
As different requirements of strain for N- or P-type transistors e.g. along the direction of the channel, the characterization of strain in electronic devices is necessary, both for monitoring the intended engineered strain but also the unintended strain states. Since in modern FDSOI technologies and other related transistor technologies the feature sizes such as channel length and thickness are typically in an order of nanometers, the strain characterization requires high spatial resolution. Such strain mapping with high spatial resolution combined with high precision can be achieved via (scanning) transmission electron microscopy (STEM).
In this work, two techniques: the precession electron diffraction (PED) and the nano beam diffraction (NBD) are being used to investigate transistor test structures and to quantify strain states on transistor structures in a 22nm Fully Depleted Silicon-On-Insulator technology. After a motivation on strain engineering in semiconductor devices the working principle as well as the measurement setup of the applied techniques shall be introduced. Finally the aim is to present recent findings of strain mapping experiments on GLOBALFOUNDRIES' current technology achieved by the presented measurement methods as is shown in figure 1 for just one example for a common pMOS structure. In order to demonstrate strain as an important performance knob strain measurements are also being related with electrical device measurements. Certain differences between these methods, e.g. in terms of accuracy, resolution, capability and time-efficiency will be pointed out.

Fig.1: TEM micrograph with an overlay strain map of the xx-component of the strain tensor (channel direction) of a standard pMOS transistor of GLOBALFOUNDRIES' 22FDX technology.

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